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Roland Boss DR-110 Dr Rhythm Graphic
SERVICE MANUAL DOCUMENTS
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From the DR-110 Information Homepage @
http://members.aol.com/leviathant/dr110.html

Since you've taken the time to read this, I'd much appreciate it that if you do some kind of nifty (or even minimal) modification to the DR-110, please email me and let me know what you've done, and if you'd be so kind to provide schemes and/or instructions as a sort of 'thanks for letting me have the DR-110 schemes Matt' kind of gesture. Please send em to levithnt@nfdc.net and let me know if you would mind if I posted them publicly on the same web site that these schemes are available from. Enjoy, happy modding!

Oh, here's the parts list, painstakingly hand typed by myself.

IC____________________-

15179122	HD44790a44P	2k x 4bit CMOS CPU with LCD driver
15179305	(mu)PD444C	1k x 4bit static RAM
15159140h0	HD14006BP	18-bit static shift register
15159104h0	HD14011BP	quadruple 2-input NAND gate
15159116TO	TC4069UBP	Hex inverter
15159117H0	HD14070bp	quadruple exclusive-OR gate
15189102	NJM4558DD	OP amp (pcb 2291084302-UP)
15199521	M51501L Power amp (pcb 2291084302-UP)	
15199517	LM-386N-1	Power amp (pcb up to 2291084300)

TRANSISTOR_________________-

15119125	2SA1115-F
15119602	2SB647-C
15119607	2SB642-R
15129137	2SC2603-F
15129145	2SC945-K (or 2SC1815-BL)

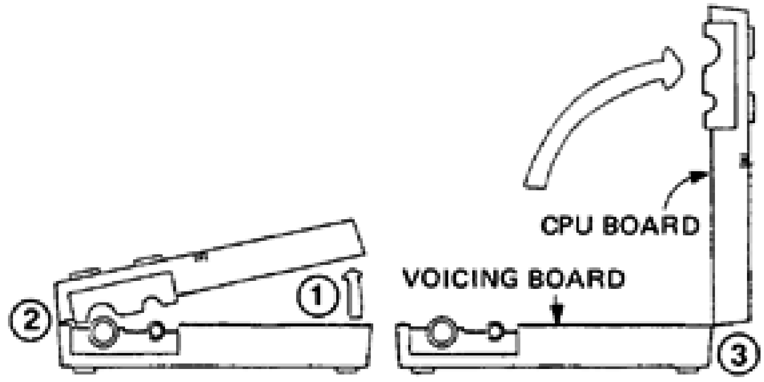
DIODE___________________

15019125	1ss-133	
15019530	s5500g	
15129137	RD6.8eb-2	zener
15019138	DAN 201 diode array	
15019139	DAP 201 diode array	

DISASSEMBLY

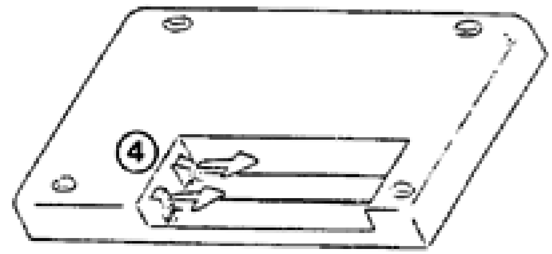
Exposing PCBs

1. Remove 4 rotary knobs.
2. Remove 3 x 12mm P type screws on Bottom case.
3. Open Top case, first at the rear end ①, gently push rearwards (unlock), then open at the front end ②. Insert a cloth between panels to protect the rear surface of top panel from scratching. This allows troublshooting for both PCBs while maintaining the unit operative from built-in drycells.



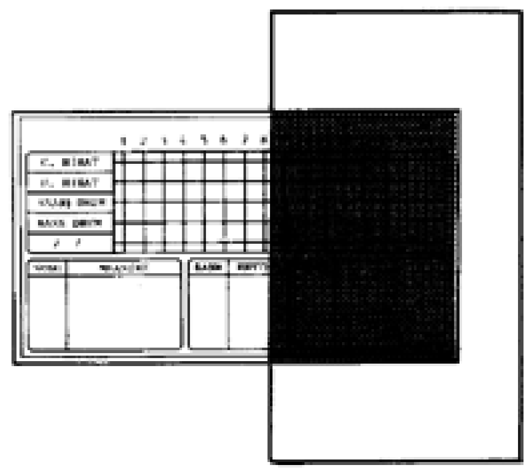
Dismounting VOICING Board

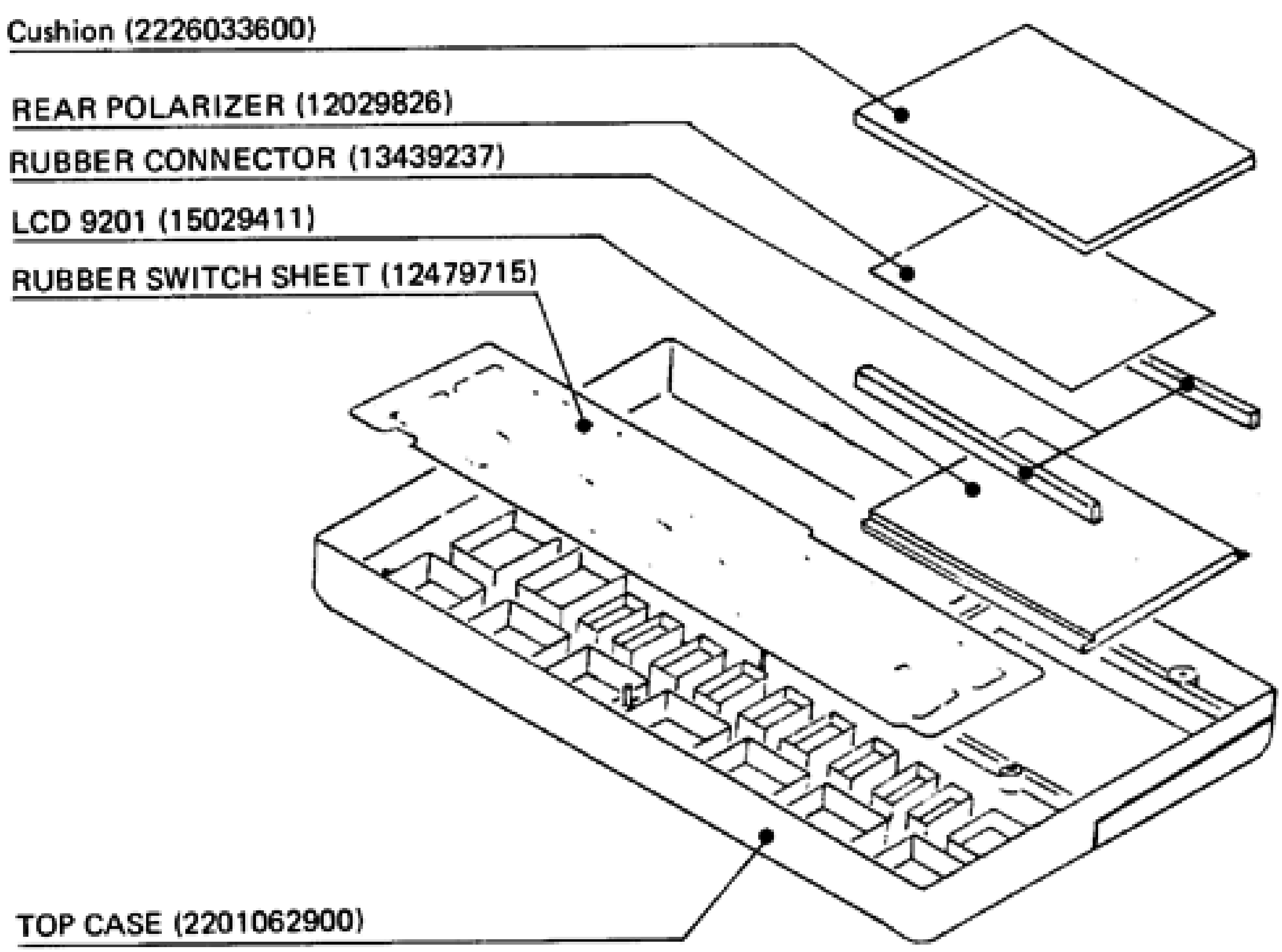
1. Remove Battery compartment cover and remove the dry cells.
2. Unlatching Battery clips ④, raise Bottom case.



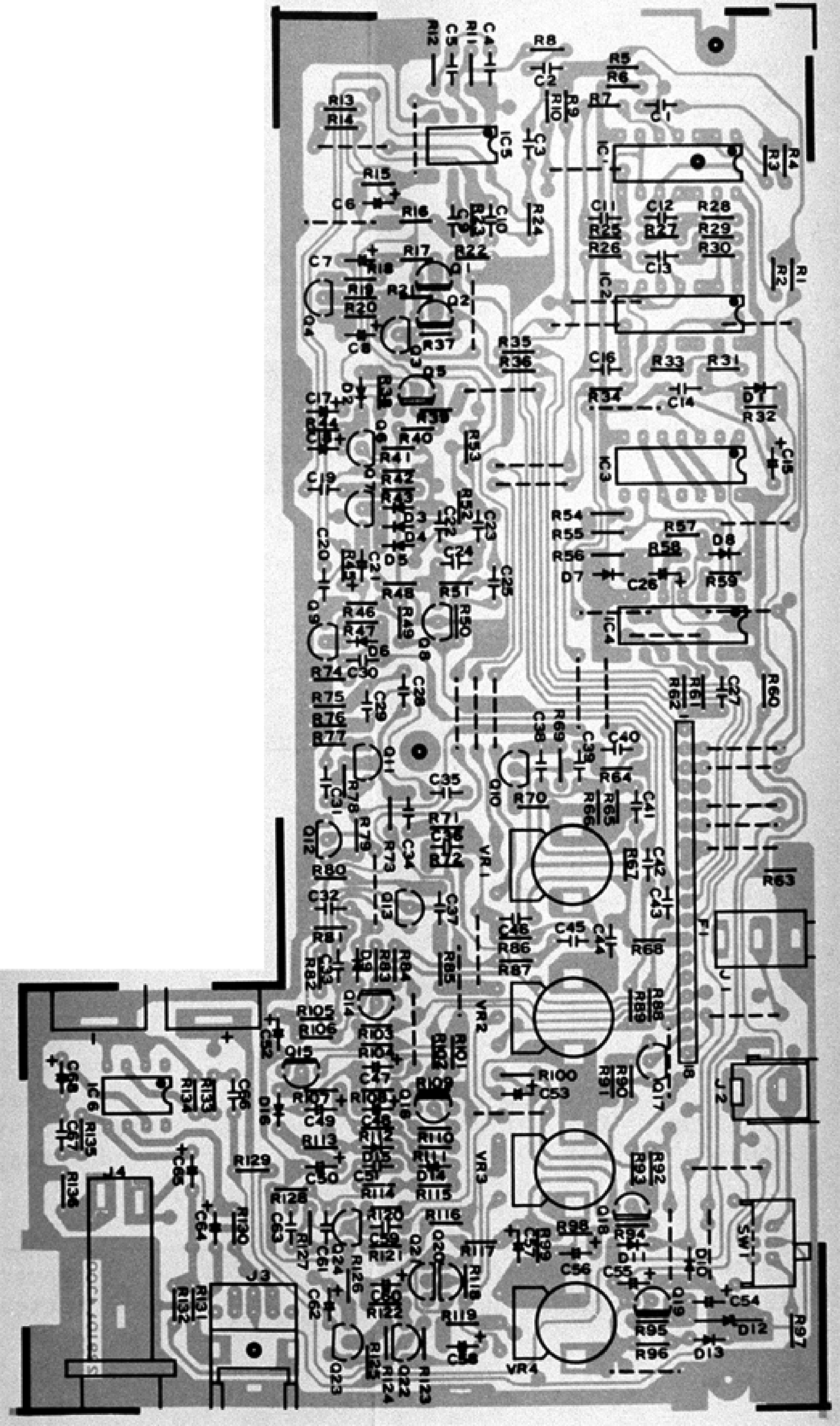
LCD ASSEMBLY

Avoid unnecessary service to LCD Ass'y,
When reassembling, make sure that the face (not rear) of Rear Polarizer touches LCD.
The correct layer makes display dark when the LCD and polarizer are placed crosswise.

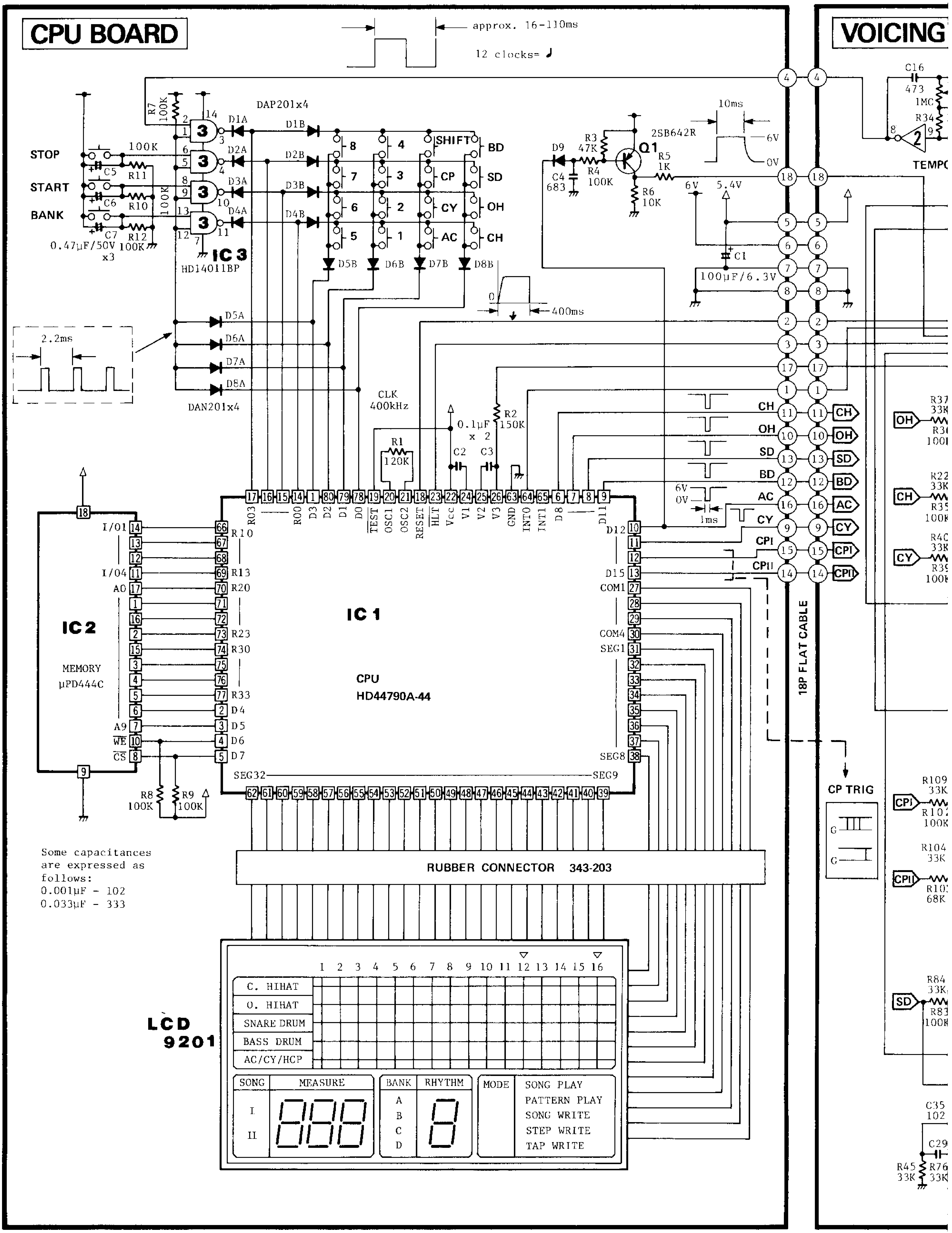



7313204006
(pcb 2291084300)
SN up to 361000

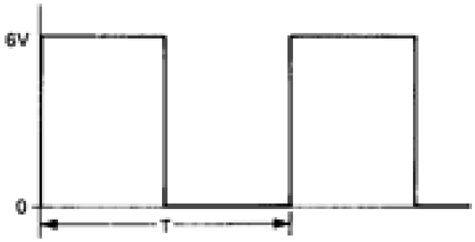


DR 110 CIRCUIT DIAGRAM

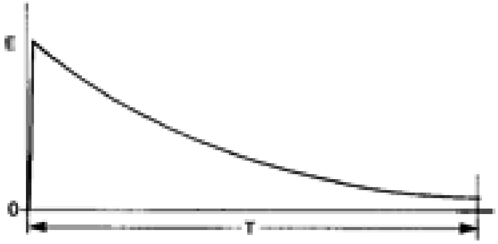



VOICING BOARD
CY SOURCE
HD14006BP
NOISE
NJM4558
TEMPO CLK
VR1
IC1
HD14069BP x 2
IC2
INT CLK
2.2ms
IC3
NC.2.8.11
POWER ON
RESET
13μs
80kHz
HD14070BP
IC4
IC1—4
Vcc
GND
0.5Vp-p
ACC TRIG OUT
J1
SW1
SSS522
RD6.8EB2
DC9V
J2
S5500G
1.5V x 4
VV +6V
VL +6V
VB 5.4V
OH
CH
SD
BD
AC
CY
CPI
CPII
18P FLAT CABLE
CP TRIG
VR2
BALANCE
20KB
VOLUME
VR4
50KA
VR3
ACCENT
1MC
(P-BUS)
OUTPUT
SN up to 361000
J4
OPHONES
J3
LM386N-1
Pins 1.8 NC
2SC945K or
2SC1815BL
Unless otherwise specified:
NPN transistors are 2SC2603F
PNP transistors are 2SA1115F
Diodes are 1SS133

WAVEFORMS

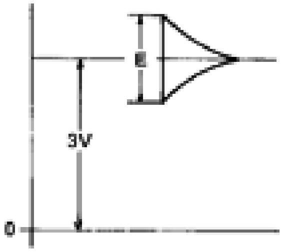


Check Point	T
1	0.87ms
2	1.22ms
3	3.15ms
4	2.15ms



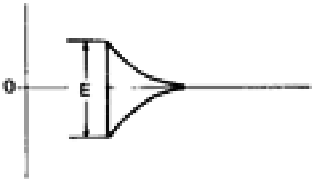
Check Point	T	E
5	700ms	6V
6	80ms	6V
7	60ms	6V
8	900ms	6V
9	1.4s	2.7V
11	140ms	5V
12	700ms	5V
13	100ms	5.7V
14	120ms	5.7V

VOL. MAX



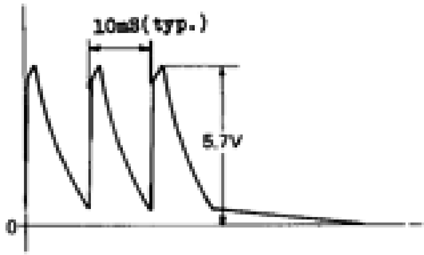
Check Point	ACCENT	E
15	MIN	1.5V
	MAX	4.5V

VOL. MAX



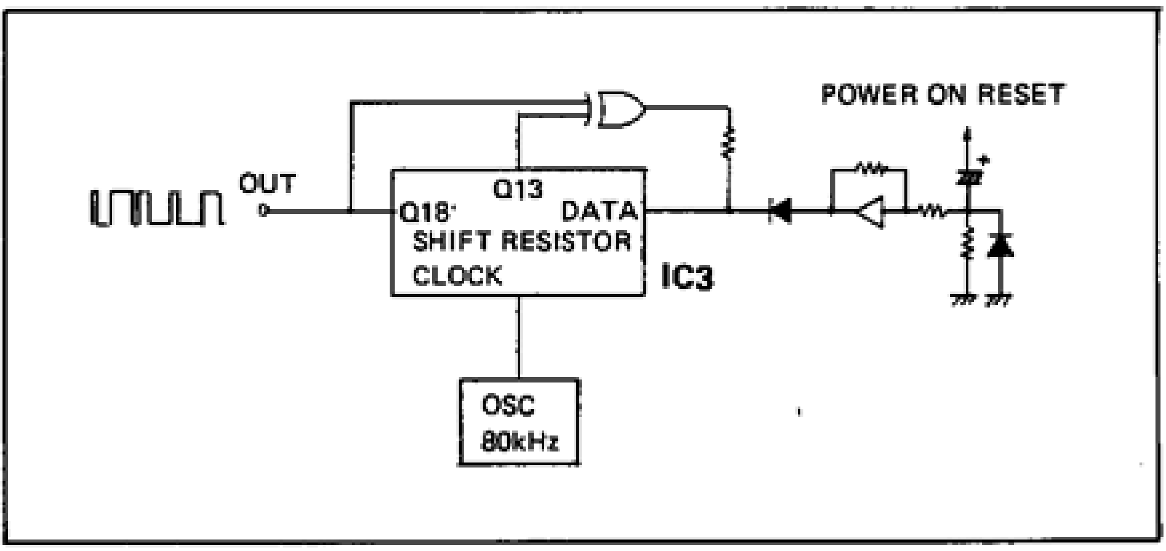
Check Point	ACCENT	E
16	MIN	0.8V
	MAX	1.9V

CP1



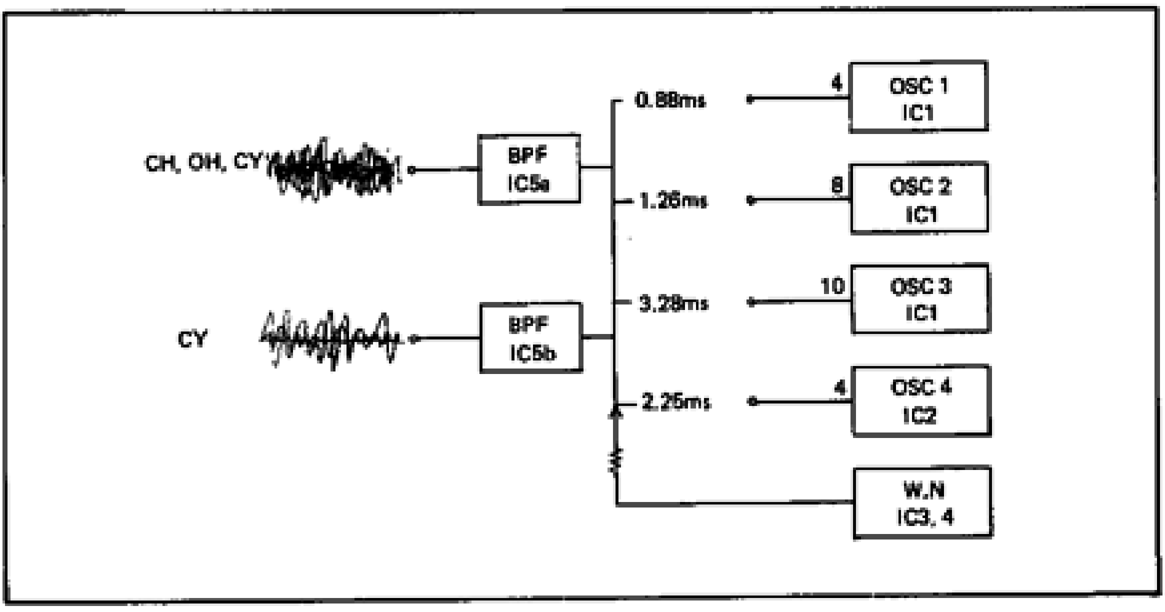
Check Point 10

NOTE: Intermitent DC supply (such as loose AC adaptor or battery connection or quick turning OFF-ON of the power switch) may upset Power—ON Reset when a transient of DC voltage is shorter than the time constant of RESET circuit. The resultant will be loss of noise sound.



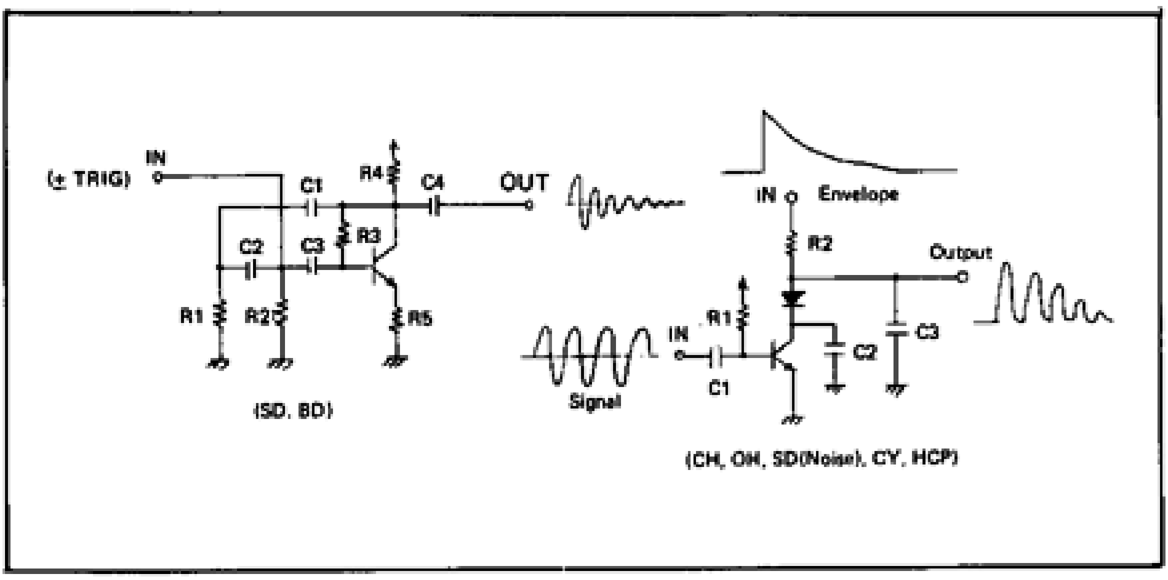
CY SOUND GENERATOR

Four generators oscillate at different frequencies which are determined based on analyses of live symbal sounds. Interrelations between frequencies are so critical that slight deviation of one frequency can cause beat sound or distortion. To let the generators stay in a specific frequency, C1, C4, C12 and C13 should be less than 5%(J) of tolerance.



VOICE GENERATORS

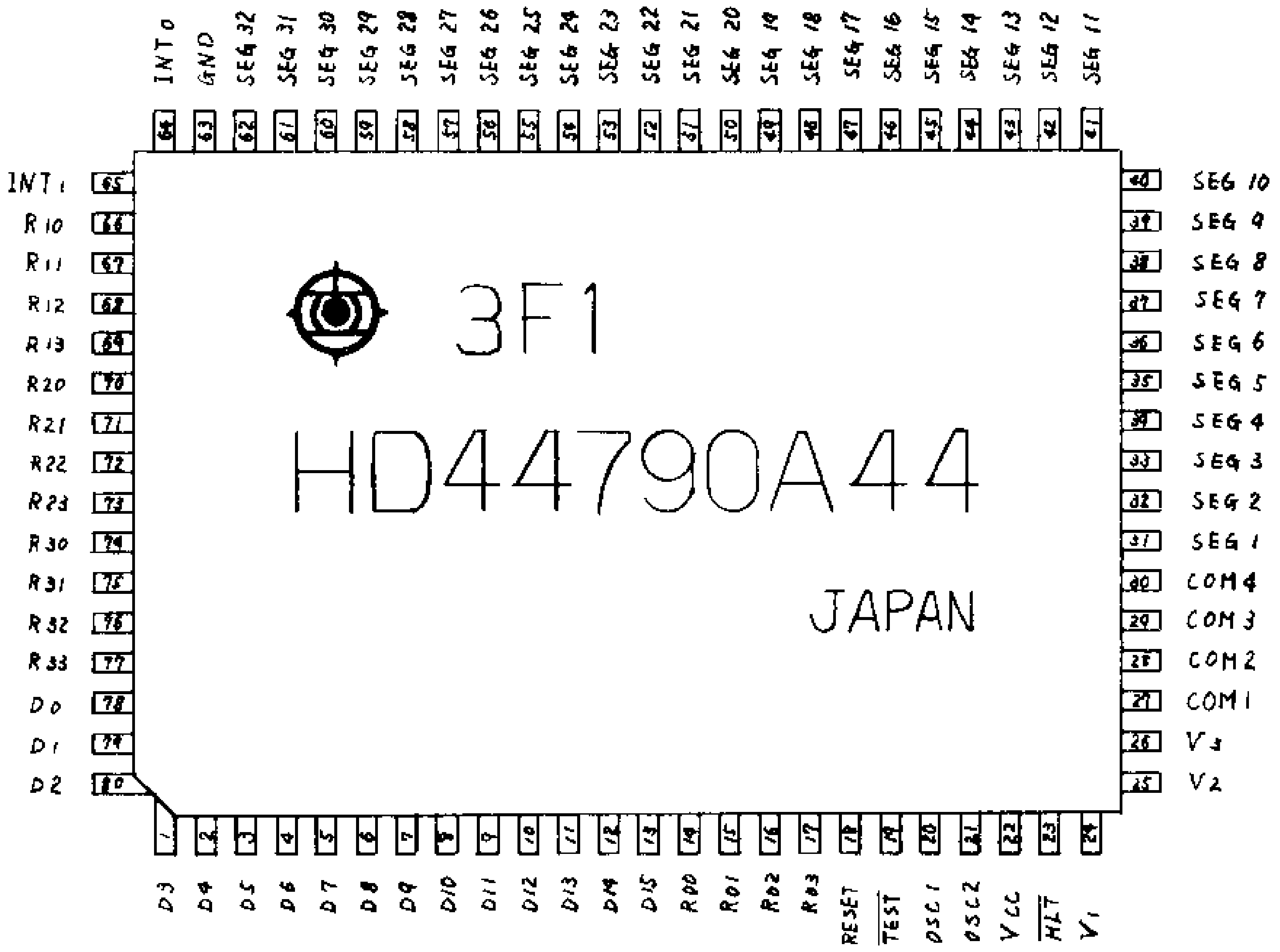
The voice generators are categorized into two groups: Damping oscillator for drum sound and a combination of Swing type VCA and Envelope generator for metalic sounds.



CIRCUIT DESCRIPTIONS

CPU IC1

HD44790A44 is a 2K word by 4 bit one chip CMOS microcomputer equipped with internal LCD drivers.



CPU HD44790A-44 PIN FUNCTIONS

Symbol	Name	Description	
R00 R01 R02 R03	Input Port	Read in Key switches and TEMPO CLOCK.	
R10 R11 R12 R13	I/O Port	External Memory Data Bus (Rhythm patterns A/B, Songs I/II)	
R20 R21 R22 R23	I/O Port	External Memory Address Bus P20–P23: Used as OUTPUT Port.	
R30 R31 R32 R33	Output Port	External Memory Address Bus P20–P23: Used as OUTPUT Port.	
D0 D1 D2 D3	Descrete I/O terminals	Output Switches and Tempo Clock Scanning signals.	
D4 D5	Descrete I/O terminals	External Memory Address Bus	
D6	Descrete I/O terminals	$\overline{WE}$ Memory Write Enable	
D7	Descrete I/O terminals	$\overline{CS}$ Memory Chip Select	
D8 D9 D10 D11 D12 D13 D14 D15	Descrete I/O terminals	CH OH SD BD AC CY CPI CPII	Output Trigger pulse to VOICEs.
INT 0 INT 1	Interrupt Inputs	Interrupt Input for Switch Scanning OPEN-pulled up internally	
RESET	Reset Input	Accepts 400ms-width pulse on Power-up.	
$\overline{HLT}$	Halt Input	When "low", the CPU retains all internal circuit status as they are.	
$\overline{TEST}$	Test Input	No customer usable terminal.	
V1 V2 V3	LCD DC Supply Inputs	Used as LCD driver signals.	
Vcc	DC Supply Input	+5V (±10%) also used as LCD DC supply	
GND	Ground Input	GND	
SEG 1 | SEG 32	SEGMENT Outputs	Output LCD drive signals	
COM 1 | COM 4	Common Outputs	Output LCD drive signals in 1/4 duty, 1/3 bias.	

SWITCH MATRIX (See Fig. below)

① The CPU enters external interrupt routine on a rising edge of INT CLK from IC2a, b which also serve as a part of CY Sound Generator, and reads in TEMPO CLK and key switches through ports D0–D3 and through R00–R03.

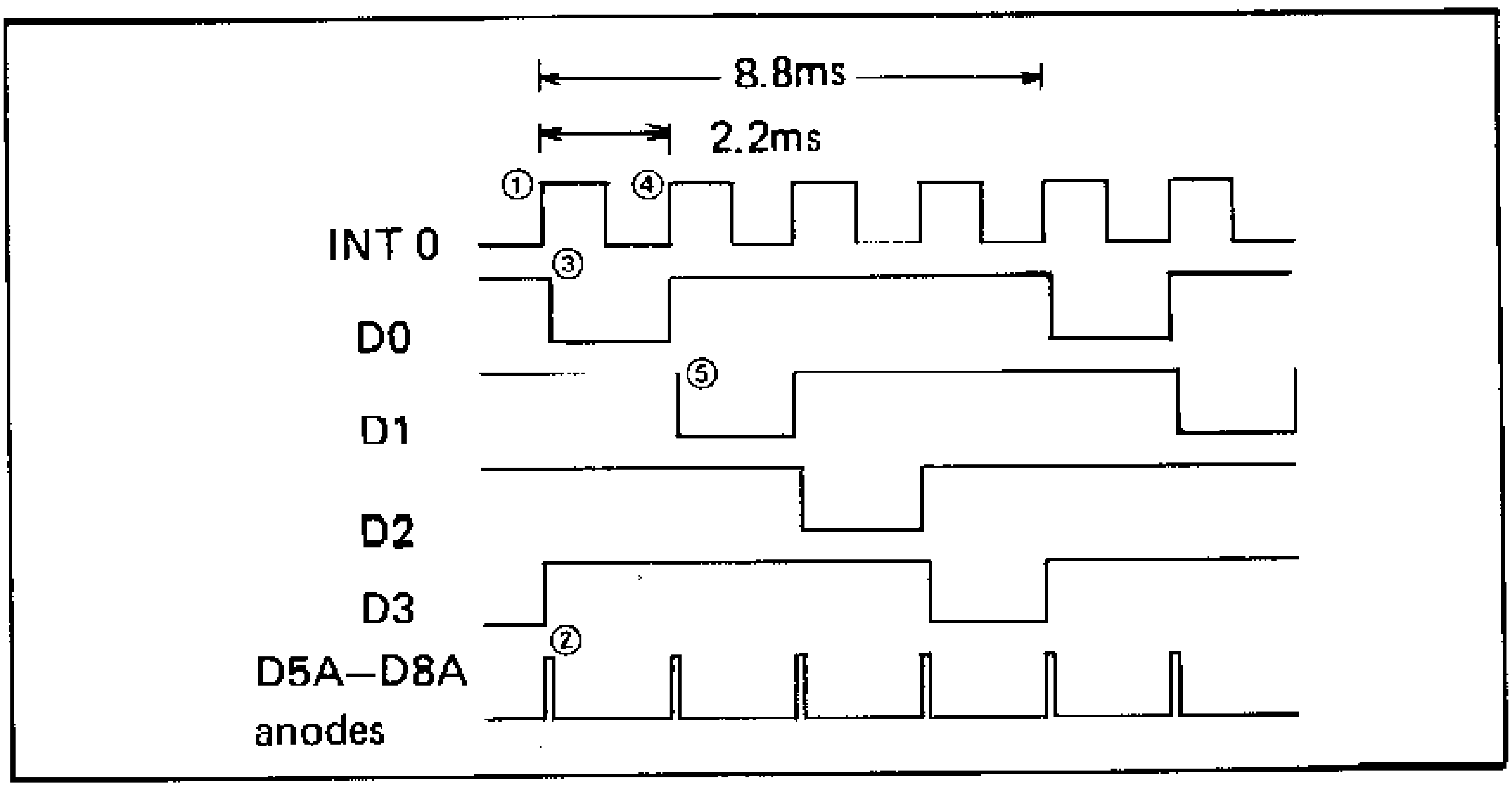
② In reading the aboves, the CPU first turns ports D0–D3 "H", cutting off D5A–D8A, D5B–D8B and D1B–D4B, disconnecting the diodes from IC3 NAND gates and the ports R00–R03. With an H being applied on one input pin, each gate of IC3 will turn its output to "L" when the other input pin is H (closing of STOP, START or BANK, or during H period of TEMPO CLK). Ports R00–R03 are pulled up internally and go low when their mate IC3 outputs turn to L.

③ Next, the CPU IC1 sets port D0 to "L" which pulls one inputs of IC3 down to low, turning all IC3 outputs to "H", reverse biasing D1A–D4A which in turn isolate IC3 from the read-in ports. Each of ports R00–R03 can be connected to port D0 through closed contacts (of CH, OH, SD or BD) and through D8B. Then the program returns to the main routine.

④ On the next rising edge of INT CLK, the program enters interrupt routine again and gates IC3.

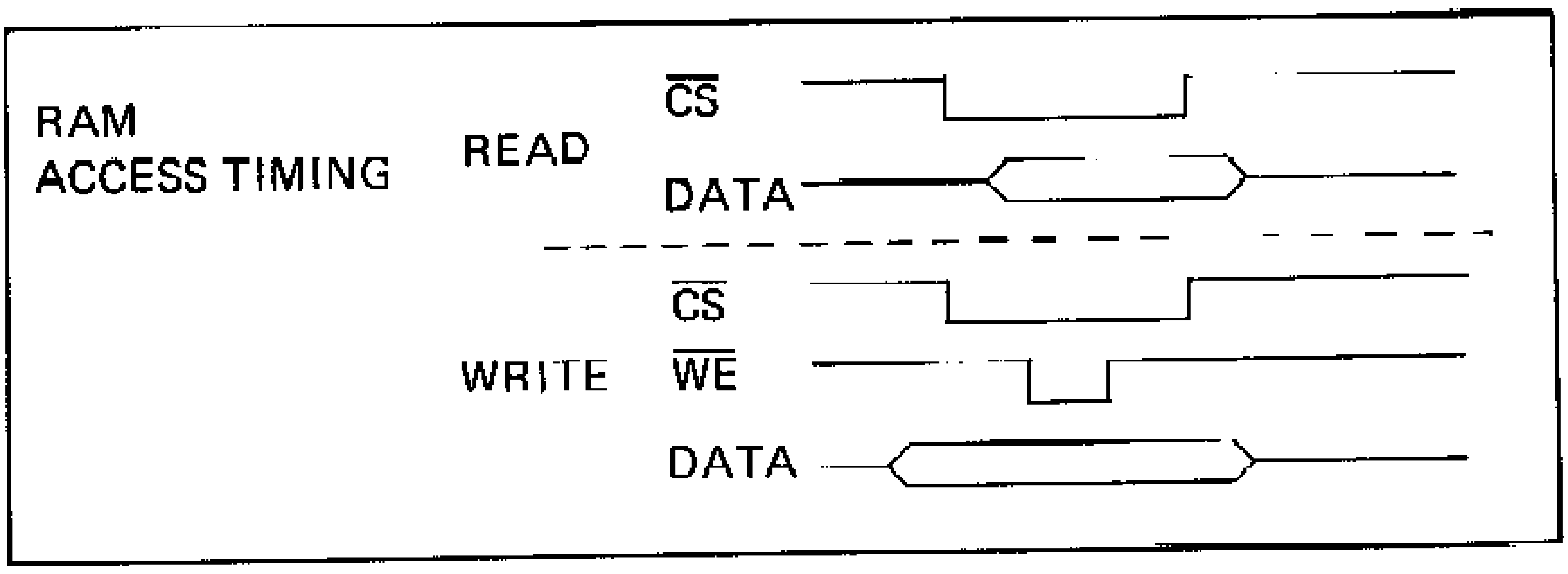
⑤ Having reading IC3 outputs, this time the program sets D1 to L and reads SHIFT, CP, CY and AC switches through R0 ports.

The CPU repeats the same procedures for the remaining D ports and returns to ①, cycling TEMPO CLK, STOP, START and BANK readings at 2.2ms internals, and other switch groups at 8.8ms intervals.



MEMORY BACKUP

IC2 μPD444C is a 1K-word by 4 bits static RAM. It is used in DR-110 for storing BANKs A/B, SONGs I/II and STEPs 12/16 data. (BANKs C/D containing factory-set rhythms are stored into CPU's internal ROM.) The RAM memory is backed up by built-in battery which bypasses power switch and connects to RAM's VCC, $\overline{WE}$ and $\overline{CS}$ pins.



During the power OFF $\overline{HLT}$ pin of IC1 CPU is kept L, maintaining all its input and output pins high impedance, isolating its circuits from peripheral circuits and thus retains all the data so far obtained. When the CPU is repowered, it initializes internal circuits but still keeps some data intact.